WHAT IS CLAIMED IS:

1. A method comprising:
generating a first clock signal with a first frequency; and
utilizing said first clock signal to generate a second clock signal with a second frequency;
wherein said second clock frequency is generated by dropping selected pulses of said first clock signal.

2. The method of claim 1, wherein utilizing said first clock signal comprises using said first clock signal to select a sequence of values from a storage element.

3. The method of claim 2, wherein said storage element comprises a first and second shift register, and wherein said sequence of values are alternately selected from said registers.

4. The method of claim 1, further comprising:
counting sequences of pulses of said first clock signal; and
detecting said selected pulses of said first clock signal.

5. The method of claim 4, wherein said sequences include a fixed number of pulses, and wherein said selected pulses correspond to particular counts of said pulses within said fixed number of pulses.

6. The method of claim 3, further comprising changing a contents of at least one of said registers at a selected time in order to generate said second clock signal with an increasing frequency.

7. A clock circuit comprising:
a first circuit configured to generate a first clock signal; and
circuitry configured to utilize said first clock signal to generate a second clock signal with a second frequency, wherein said second clock frequency is generated by dropping selected pulses of said first clock signal.

8. The clock circuit of claim 7, further comprising a storage element configured to store a pattern of bits, wherein said circuitry is configured to utilize said first clock signal to select a sequence of values from a storage element.

9. The clock circuit of claim 7, wherein said storage element comprises a first and second shift register, and wherein said circuitry is configured to select said sequence of values from said registers in an alternating manner.

10. A system comprising:
a reference clock generator configured to generate a reference clock signal; and
a processor comprising a clock circuit configured to:
receive said reference clock signal;

generate a first clock signal from said reference clock signal; and

utilize said first clock signal to generate a second clock signal with a second frequency, wherein said second clock frequency is generated by dropping selected pulses of said first clock signal.